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1. JP401284959A , Nov. 16, 1989, COMMON MEMORY ACCESS SYSTEM; MURAOKA, YASUTOKI,
INT-CL: G06F15/16; G06F13/16; G06F13/18

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JP401284959A Nov. 16, 1989 L3: 1 of 1

COMMON MEMORY ACCESS SYSTEM

INVENTOR: MURAOKA, YASUTOKI
APPLICANT: NEC CORP
APPL NO: JP 63115835
DATE FILED: May 11, 1988
INT-CL: G06F15/16; G06F13/16; G06F13/18

ABSTRACT:

PURPOSE: To minimize the increase of the processor waiting time in a common memory access system by shortening the cycle time of a memory circuit.

CONSTITUTION: A bus controller 4 ensures the **arbitration** between the **request** signals RQ received from two processor interface circuits 31 and 32 and then selects the circuit 31 with an enable signal EN via an **arbitration** bus 61. Then the circuit 31 sends an address signal AD to the controller 4 via a **unidirectional** **bus** 51. The controller 4 receives the signal AD from the circuit 31 and sends this signal to a memory circuit 1 via a directional bus 2. At the same time, the signal EN showing the permission for reception is sent to the circuit 31 under access via an **arbitration** bus 62. Thus the cycle time is shortened with use of two **unidirectional** **buses** 51 and 52 having different directions of transmission.

d 1-9 cit ab

1. 5,758,109, May 26, 1998, Repeater/switch for distributed arbitration digital data buses; Thomas Austin Gafford, et al., 710/128, 129 [IMAGE AVAILABLE]

US PAT NO: 5,758,109 [IMAGE AVAILABLE] L3: 1 of 9

ABSTRACT:

The technical field of the invention generally concerns digital computers and, in particular, repeaters or switches (40) for distributed **arbitration** digital data buses (52, 54, 56, and 58) to which devices (62, 64, 66, 68, 72 and 74) connect in parallel. The bus repeater/switch (40) includes a plurality of bus interface cards (48) that are connected to the distributed **arbitration** buses (52, 54, 56 and 58) for receiving signals from and transmitting signals to devices (62, 64, 66, 68, 72 and 74) connected thereto. The bus interface cards (48) connect to a control card (44) which allows signals from one of the sharing buses (52, 54 or 56) to be exchanged with the shared bus (58). The bus switch (40) also includes selector switch (84 or 88) for choosing which particular one of the sharing buses (52, 54 or 56) exchanges digital data signals with the shared bus (58). The bus switch (40) responds to signals on the distributed **arbitration** buses (52, 54, 56 and 58) and to phases of the protocol for those signals so that its presence between pairs of buses (52-58, 54-58 or 56-58) is imperceptible to devices (62, 64, 66, 68, 72 and 74) connected thereto.

2. 5,689,657, Nov. 18, 1997, Apparatus and methods for bus arbitration in a multimaster system; Hans-Jurgen Desor, et al., 710/119, 107, 242 [IMAGE AVAILABLE]

US PAT NO: 5,689,657 [IMAGE AVAILABLE] L3: 2 of 9

ABSTRACT:
A bus **arbitration** method for a multimaster system comprising a plurality of masters sharing a global data bus and a plurality of bus **arbiters** sharing a global identification bus. Each active bus **arbiter** applies to the identification bus a bus request signal containing a k-bit-wide identification word representative of the priority of the master associated with the bus **arbiter**. In each prioritization step of the bus grant cycle, a logic level is produced on the identification bus by logically combining bits of equal significance. This logic level is then compared with the corresponding bits of the applied identification words. The k bits of the identification words of the bus **arbiters** are placed on the identification bus on a time-graded basis; in each prioritization step of the bus grant cycle, only those bits of the identification words are placed on the identification bus which are of equal significance, and in each prioritization step of the bus grant cycle, those bus **arbiters** whose identification word bit in the prioritization step does not match the logic level of the identification bus are eliminated from the bus **arbitration** of the bus gram cycle.

3. 5,684,966, Nov. 4, 1997, Method for operating a repeater for distributed arbitration digital data buses; Thomas Austin Gafford, et al., 710/129, 2, 131; 711/147 [IMAGE AVAILABLE]

US PAT NO: 5,684,96[illegible] [IMAGE AVAILABLE] L[illegible]3 of 9

ABSTRACT:
The technical field of the invention generally concerns digital computers and, in particular, repeaters or switches (40) for distributed **arbitration** digital data buses (52, 54, 56, and 58) to which devices (62, 64, 66, 68, 72 and 74) connect in parallel. The bus repeater/switch (40) includes a plurality of bus interface cards (48) that are connected to the distributed **arbitration** buses (52, 54, 56 and 58) for receiving signals from and transmitting signals to devices (62, 64, 66, 68, 72 and 74) connected thereto. The bus interface cards (48) connect to a control card (44) which allows signals from one of the sharing buses (52, 54 or 56) to be exchanged with the shared bus (58). The bus switch (40) also includes selector switch (84 or 88) for choosing which particular one of the sharing buses (52, 54 or 56) exchanges digital data signals with the shared bus (58). The bus switch (40) responds to signals on the distributed **arbitration** buses (52, 54, 56 and 58) and to phases of the protocol for those signals so that its presence between pairs of buses (52-58, 54-58 or 56-58) is imperceptible to devices (62, 64, 66, 68, 72 and 74) connected thereto.

4. 5,621,899, Apr. 15, 1997, Switch for distributed arbitration digital data buses; Thomas A. Gafford, et al., 710/119 [IMAGE AVAILABLE]

US PAT NO: 5,621,899 [IMAGE AVAILABLE] L3: 4 of 9

ABSTRACT:
The technical field of the invention generally concerns digital computers and, in particular, repeaters or switches (40) for distributed **arbitration** digital data buses (52, 54, 56 and 58) to which devices (62, 64, 66, 68, 72 and 74) connect in parallel. The bus repeater/switch (40) includes a plurality of bus interface cards (48) that are connected to the distributed **arbitration** buses (52, 54, 56 and 58) for receiving signals from and transmitting signals to devices (62, 64, 66, 68, 72 and 74) connected thereto. The bus interface cards (48) connect to a control card (44) which allows signals from one of the sharing buses (52, 54 or 56) to be exchanged with the shared bus (58). The bus switch (40) also includes selector switch (84 or 88) for choosing which particular one of the sharing buses (52, 54 or 56) exchanges digital data signals with the shared bus (58). The bus switch (40) responds to signals on the distributed **arbitration** buses (52, 54, 56 and 58) and to phases of the protocol for those signals so that its presence between pair of buses (52-58, 54-58 or 56-58) is imperceptible to devices (62, 64, 66, 68, 72 and 74) connected thereto.

5. 5,440,698, Aug. 8, 1995, Arbitration of packet switched busses, including busses for shared memory multiprocessors; Pradeep S. Sindhu, et al., 395/200.55; 340/825.51; 364/228, 229, 229.2, 240, 240.1, 240.2, 242.6, 242.92, 260, 260.1, DIG.1; 370/462; 709/235; 710/113, 116, 128 [IMAGE AVAILABLE]

US PAT NO: 5,440,698 [IMAGE AVAILABLE] L3: 5 of 9

ABSTRACT:
An **arbiter** is provided for resolving contention on synchronous packet switched busses, including busses composed of a plurality of pipelined segments, to ensure that all devices serviced by such a bus are given fair, bounded time access to the bus and to permit such devices to fill all available bus cycles with packets. Flow control for shared memory multiprocessors is readily implemented with this **arbiter** because the **arbiter** supports different types of **arbitration** requests and the prioritization of such **arbitration** requests by type.

6. 5,339,404, Aug. 16, 1994, Asynchronous TMR processing system; Gilbert C. Vandling, III, 714/12, 820 [IMAGE AVAILABLE]

US PAT NO: 5,339,40[redacted] IMAGE AVAILABLE] [redacted] 6 of 9

ABSTRACT:
A triple modular redundancy computing system including three asynchronously connected processing elements, each having its own memory, a plurality of **arbiters** cross connecting processor elements for enforcing synchronization for tasks and for voting **arbitration** on output and without voting for inputs.

7. 4,977,494, Dec. 11, 1990, High speed digital motion controller architecture; John B. Gabaldon, et al., 364/167.02; 318/568.2; 364/132, 474.11; 395/84 [IMAGE AVAILABLE]

US PAT NO: 4,977,494 [IMAGE AVAILABLE] L3: 7 of 9

ABSTRACT:
A system bus (13) carrying multidimensional path data interfaces with a plurality of local microprocessors (24), one for each dimension, through a plurality of dual access memory structures (21), one for each local microprocessor (24). A local **arbiter** (35) controls access to each dual access memory structure (21), facilitating elimination of wait states in data transfers between the bus (13) and memory (21) and between the local microprocessor (24) and memory (21). The **arbiter** (35) is implemented using a programmable logic device state machine approach, which implements a mode of operation wherein the circuitry is armed for a transfer between a local microprocessor (24) and the dual access memory (21) and accomplishes such transfer with no wait states. The state machines and dual access memory (21) are driven by a clock which is twice as fast as that driving the local microprocessor (24) and the state machine implementation utilizes this fact to insure memory access to both the system bus (13), and the local microprocessor (24) with priority going to the local microprocessor (24).

8. 4,803,617, Feb. 7, 1989, Multi-processor using shared buses; Thomas N. Berarducci, 395/800.11; 364/230.6, 231.9, 232.8, 237.8, 237.82, 237.9, 239, 239.7, 240, 240.2, 242.6, 242.91, 242.92, 260, 260.2, 264, 264.6, DIG.1; 712/14 [IMAGE AVAILABLE]

US PAT NO: 4,803,617 [IMAGE AVAILABLE] L3: 8 of 9

ABSTRACT:
A multi-processor apparatus is disclosed which includes an array of separately addressable memory units and an array of separately addressable processors. A first unidirectional bus delivers data from a selected processor to a selected memory unit. A second unidirectional data bus delivers data from a selected memory unit to a selected processor. **Arbitor** circuits control the flow of data to these data buses.

9. 4,470,114, Sep. 4, 1984, High speed interconnection network for a cluster of processors; Mark L. C. Gerhold, 710/111; 364/221, 221.5, 228.5, 229, 229.2, 229.3, 229.4, 231.4, 231.7, 232.8, 238, 238.5, 239, 239.8, 240, 240.1, 240.5, 240.8, 241.1, 241.2, 241.3, 241.9, 242.31, 242.6, 242.9, 242.92, 242.94, 256.3, 256.6, 260, 260.1, 260.2, 263, 271.6, 271.8, 280, 281.3, 281.4, 284, 284.4, DIG.1 [IMAGE AVAILABLE]

US PAT NO: 4,470,114 [IMAGE AVAILABLE] L3: 9 of 9

ABSTRACT:
A high speed interconnect network for a relatively large number of processors from as few as five to a hundred or more where the information transfers are serial-by-byte in a time multiplexed manner so that when one or more processors is ready to transmit, there will be an information byte being transmitted every clock time. A bus **arbiter** controls

access to a local bus in a round-robin fashion when one or more than one processor is requesting access to the local bus. The bus arbiter also serves for connection to an overall global loop of bus arbiters each of which has a local bus and a plurality of individual processors.